

An Efficient On-line Monitoring BIST for Remote Service System

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Abstract. Home networking has been developing rapidly due to the increase of the internet users and the advent of digital economy. In this context, the quality and service under guarantee for internet intelligence electric home appliances has become quite important. Therefore, to guarantee the performance of the appliances, on-line testing for detecting latency faults should be performed. In this paper, we develop a new efficient architecture of on-line BIST. In addition we propose a remote service system for CSM (Customer Satisfaction Management) based on home networking.

Key Words: on-line monitoring, test, remote service system, BIST

1 Introduction

Recently, the worldwide population of internet users is increasing rapidly, which leads to new trends such as the extension of supplying multi-PC for domestic use and the fusion of telecommunication and electric home appliances, etc. Hence a need for Internet intelligence electric home appliances is rising and internet application field is expanding from computers to electric home appliances. Therefore, home networking industry has developed recently more than 15% in the worldwide market, which is causing tremendous far-reaching effects on economy. Now, home networking is an important issue in the information technology field[1][2]. Home networking provides home electric appliances which have more intelligent functions and higher performance. However, consumers demand more reliable appliances and more convenient service under guarantee. Therefore rigorous testing becomes more important to assure the quality and service of home appliances. There are two kinds of testing, off-line testing and on-line testing. The former means that the testing is performed while the system is not operating, and the latter means that the testing is performed during system operation. Usually off-line testing is used to improve the quality by not shipping products which have defects. However using on-line testing, the service costs which include parts and labors can be reduced. In addition, the improvement of service quality can greatly encourage purchasing power of the customers[3]. In this paper,

we develop a new efficient architecture of on-line BIST (Built-In Self Test) for identifying faults during system operation. This can be used in a remote service system based on home networking.

2 Remote service system

To construct an efficient remote service system, several things should be considered. Firstly DFT(Design for Testability) should be considered from the beginning. We can find errors of the designs and follow the systematic designs efficiently using DFT. Secondly, suitable test processes should be followed. There are two kinds of test processes: off-line testing and on-line testing. Off-line testing detects the faults caused during the manufacturing process. On the other hand on-line testing detects the faults caused by defective operations and bad effects from the outside during operation. To apply off-line testing, BIST and/or tester can be used. On the other hand, on-line testing must use BIST. Thirdly, the network which connects all systems should be formed. Finally, the databases obtained from the analysis of the test information should be prepared[4][5]. The system constructed with the above design, has many advantages. Especially with on-line BIST, not only the latency faults that can't be detected by off-line testing are found but also the service is improved by repairing the faults detected by on-line BIST. Suppose that there is a defect in a refrigerator. It is detected by on-line BIST before the consumer finds out. And this information will be sent to the manufacturing company via internet and the message is sent to the user via e-mail or SMS (Short Message Service) at the same time. Next, the company analyzes the problem. Then the process of repairing or exchanging parts

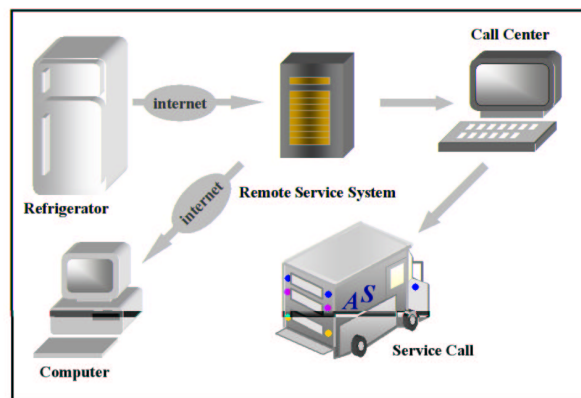


Fig. 1. Example of the remote service system

is followed. All these steps are shown in Figure 1. Consequently, the concept of the "intelligent service under guarantee" can be constructed based on the remote service system. This concept means that the service centers provide maintenance service for home appliances before the consumers ask for it. This system has a number of advantages: the cost of service can be reduced, high quality of service can be provided and the quality of products can be improved.

3 Effective on-line monitoring architecture

3.1 Overview of on-line monitoring system

There are two kinds of on-line testing. One is inserting additional testing modes and the other is on-line monitoring [6]. Inserting additional testing modes between normal operation actions is illustrated in Figure 2. This method has a

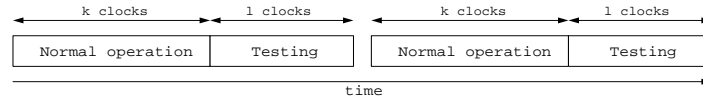


Fig. 2. Overlapping of testing and normal operation on the CUT

merit that it could apply deterministic test patterns which have high fault coverage through additional test modes. But it is difficult to determine when the test modes are inserted. In other words, it is difficult to estimate when system blocks enter into the idle time from normal operation and how long the idle time is continued. Therefore, it is not easy to use this method. On the contrary, on-line monitoring BIST determines whether the system has faults or not by comparing a monitored event come out from the functional input with an estimated operating result of the fault free system. For example, let's look at on-line monitoring pipelined function block shown in Figure 3. In this case, on-line monitoring circuit has a trait that a signal appears at the input terminal and after four clocks the specific signal combination appears at the output terminal. Therefore in a fault free situation, it is possible to predict an output signal combination after four clocks by monitoring the input signal combination. OMB(On-line Monitoring Block) in Figure 3 detects a monitored signal combination and captured signal after the estimated number of system clocks. And by observing this captured signal, the defects of the on-line system are detected. This paper suggests an effective test structure and a controlling method at the on-line state.

3.2 OMB(On-line Monitoring Block)

OMB(On-line Monitoring Block) examines a input signal combination on the function block and performs a corresponding test action when the pre-determined

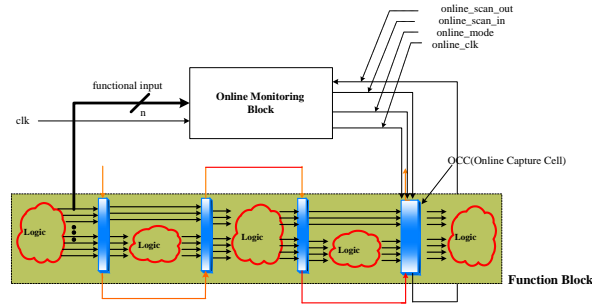


Fig. 3. Overview of on-line monitoring system

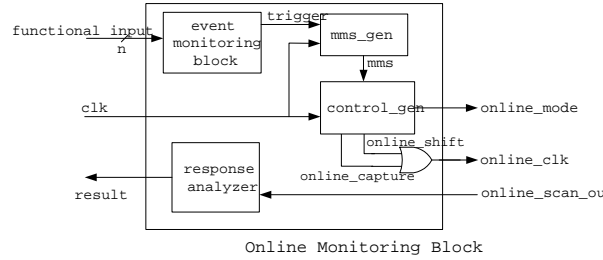


Fig. 4. On-line monitoring block

signal combination happens. OMB shown in Figure 4 regards the functional inputs and the system clock of the function block as inputs. Event Monitoring Block(EMB) observes the occurrence of the pre-determined functional input combination. We call this input combination as an ‘event’. As a result, EMB monitors the functional input combination, enables the trigger signal and has the on-line monitoring action start when the ‘event’ occurs. mms_gen is a block that generates a signal required for state changing of control_gen. control_gen is a finite state machine consisted of 4 states. It generates a control signal required by the OCC(on-line capture cell). Response Analyzer compares the signal captured by on-line monitoring actions to the signal expected in a fault free case.

Event Monitoring Block An event of EMB is selected in consideration of the function block’s feature, because the number of monitoring event determines the size of the hardware. So the input combination used frequently by the function blocks or critical to system operations is regarded as an event of EMB. At this time, there is a trade-off between the credibility of on-line operations of a system and the overhead of the hardware. That is, the more the number of events, the more credible is a system. As a result, the overhead of the hardware would increase.

control_gen The control_gen block is an FSM made up of 4 states and it changes its conditions by signal of the mms_gen block and generates the control signal on OCC. Figure 5 is a state diagram of control_gen. control_gen is made up of four

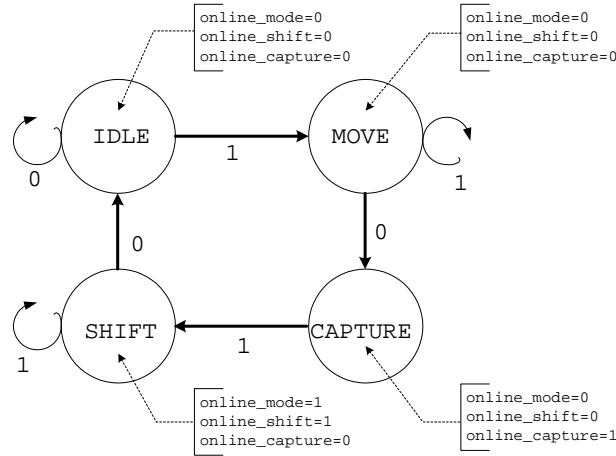


Fig. 5. State diagram of control_gen

states: IDLE, MOVE, SHIFT, and CAPTURE. Each number (0 and 1) beside states means the value of mms in clk's negative edge.

- IDLE state : IDLE state means a situation before an event is detected in monitoring block. This state is maintained by mms, which is 0 and does not generate capture or shift actions by the control signal on OCC. In this state, the function block operates only functional actions.
- MOVE state : During the process of detecting an event and transferring its result to the output, control_gen is in MOVE state. For example, like Figure 3, it takes 4 clks for the expected result to come out at the output. So control_gen is allowed to maintain MOVE state during an event propagation at the output of the function block.
- CAPTURE state : A detected event was propagated to the output of the function block and captured by the OCC.
- SHIFT state : In SHIFT state, the output captured in CAPTURE state is moved to the Response Analyzer. The value of mms in SHIFT state maintains 1.

mms_gen mms_gen is an FSM, which has 4 states and generates mms required to change a state of control_gen. Figure 6 shows a state diagram of mms_gen and Figure 7 shows an algorithm of mms_gen. mms_gen includes a num.stage register, which has information about the number of pipeline stages in the function block and num.shift register, which has information about the number of OCCs. These two registers are hardwired registers.

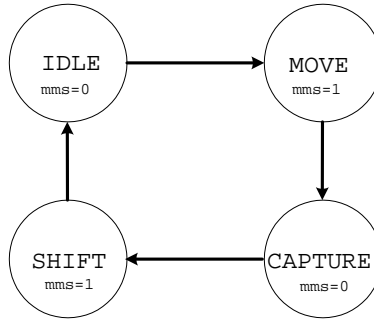


Fig. 6. State diagram of mms_gen

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algorithm mms_gen
  This algorithm generates mms (monitoring mode select) signal for control_gen
  Pre num_stage is the total number of pipeline stages of UUT
      num_shift is the total number of OCS (online capture cell) in th
      current is the state of mms_gen
  Post generate mms

  0   every posedge of clk {
  1   current = idle without any event in the trigger signal
  2   if (posedge trigger) current = move
  3   for (i=0; i != stage; i++) current = move
  4   current = capture
  5   current = shift
  6   for (i=0; i != num_shift; i++) current = shift
  7   current = idle
  8   if (current = idle) mms = 0
  9   else if (current = move) mms = 1
 10   else if (current = capture) mms = 0
 11   else if (current = shift) mms = 1 }
end mms_gen

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Fig. 7. Generation algorithm of mms signal

Response Analyzer A captured result is passed to the compression unit named Response Analyzer instead of being transferred to the external circuit directly, and a signature with a very short length is generated. And then, the signature is directly transferred to the external circuit. By doing so, we can detect malfunctions without comparing the responses of all the test patterns one by one.

3.3 OCCs(On-line Capture Cells)

OCCs that form the last pipeline stage of the function block obtain the result for a event which is passing through a circuit. In addition, the shift operation of OCCs takes place for the captured value to be observed in Response Analyzer. Figure 8 shows OCCs. As the latest ICs are more complicated, testing also

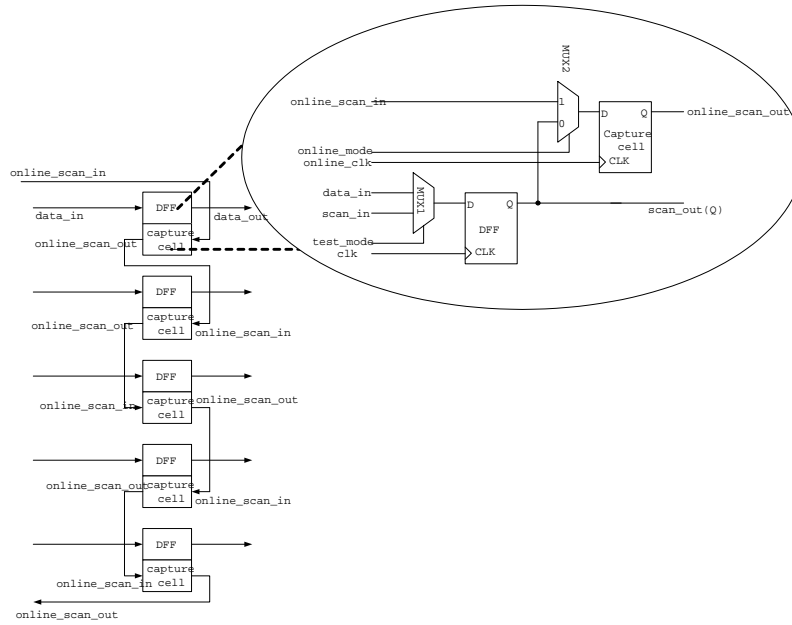


Fig. 8. OCC(On-line Capture Cell)

becomes more difficult to perform. Unless it is considered in the early design state, testing ICs might be almost impossible. Scan is a technique which replaces all flip-flops to scan cells to improve the controllability and the observability of the circuit. An OCC is a modified scan cell by adding MUX2 and a capture cell for on-line monitoring. In a state where an event is not activated, it is the same as the operation of the standard scan cell because a positive edge by the control_gen is not generated at online_clk signal. But if an event is generated in

the function block, control_gen is moved to CAPTURE state via MOVE state and online_clk makes the functional output captured in capture cell. Then the captured result moves to the Response Analyzer through the serial path in every online_clk's positive edge generated in control_gen's SHIFT state.

4 Results

In this section we model the proposed on-line monitoring architecture in HDL and perform functional verification. Figure 9 shows an example of a function block which has a latency fault. Assume that the latency fault is not detected during off-line testing and it can be modeled as a stuck-at-0 fault. Also, suppose that in the whole system the input combination of 11101 and 01010 occurs frequently according to the function of the function block. The on-line monitoring block may capture the events of 11101 and 01010 by monitoring of inputs and then it can be found out whether the function block operates normally or not.

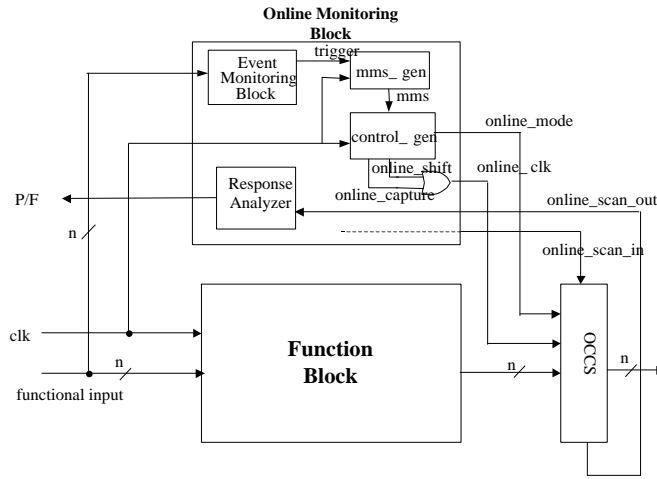


Fig. 9. Example function block

The trigger is enabled when the func_vectors are 11101(1D) or 01010(0A). After the trigger is enabled, the on-line monitoring block stays on the move state until the output signal is visible at the outputs. The response analyzer compares the expected results and the captured results. In Figure 10, the on-line captured result of the first event is 00010(02), and the result of the second is 10100(14). If the system during on-line testing is fault free, the expected results are 00010(02) and 10101(15) respectively. The simulation shows that the captured result in the second event differs from the expected result due to the stuck-at-0 fault. So the P/F indicates whether the latency fault occurs or not. Since there have been only

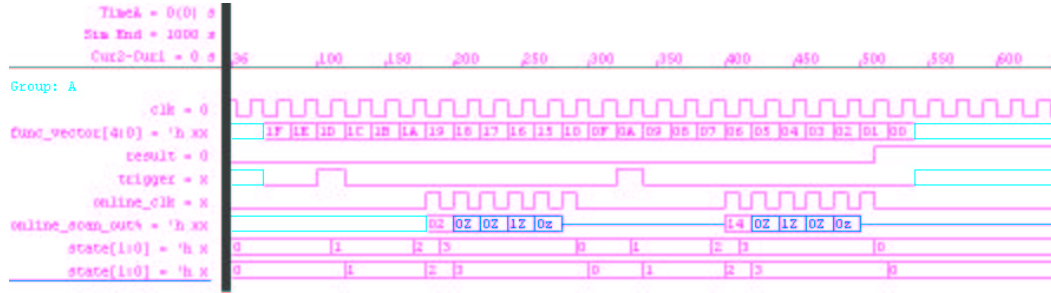


Fig. 10. Simulation result

a few researches about on-line monitoring, it is very difficult to compare the new work with the previous works. The simulation results prove that if a function block has latency faults, the proposed on-line monitoring architecture can detect its malfunction correctly. This can be used as a remote control system.

5 Conclusion

In this paper, we have proposed a new on-line BIST architecture to detect latency faults that can happen during the application of the system chip. The proposed on-line BIST architecture establishes the functional vectors that are effective for testing its operational fault as an event. The on-line BIST monitors whether the established event occurs or not, so when the event occurs, it captures the response of the UUT(Unit Under Test) during on-line testing. It also operates on-line testing that examines whether latency faults occur or not by comparing the expected outputs with the captured outputs. The new architecture minimizes the affects to the system operation due to on-line testing. The on-line monitoring technique can be applicable in many ways. Most people expect that service network will change from the existing service under guarantee system to the intelligent service under guarantee system because of the appearance of household electric goods in web application lately. Therefore the new proposed on-line BIST through on-line monitoring is very promising and has various applications.

References

1. AGRAWAL, S.K., etc: Resource based service provisioning in differentiated service networks. Proc. Of IEEE International Conference on Communications (2001) 1765–1771
2. HUANG, K.L., etc: web-based product design review: implementation perspective. Proc. of International Conference on Computer Supported Cooperative Work in Design (2001) 261 – 266
3. MARSHLL, P., etc: Home networking: a TV perspective. Electronics & Communication Engineering Journal (2001) 209 –212

4. SALZMANN, C., etc: Design for test and the cost of quality. Proc. Of International Test Conference (1988) 302–307
5. BRAUNE, D., etc: ASIC design for testability. Proc. Of ASIC Seminar and Exhibit (1989) 1–10
6. AL-ASAAD, H., etc: On-line built-in self-test for operational faults. Proc. Of AUTOTESTCON Proceedings (2000) 168–174